DURHAM COLLEGE
SUCCESS MATTERS

School of Science & Engineering Technology

DIGITAL FUNDAMENTALS I

2021-22 Academic Year

Program	Year	Semester
SET-Biomedical Engineering Technology	1	1
SET-Electromechanical Engineering Technology	1	1
SET-Electromechanical Engineering Technology (Coop)	1	1
SET-Electronics Engineering Technician	1	1
SET-Electronics Engineering Technology	1	1

Course Code:	DGFN 1131	**Course Equiv. Code(s):**	N/A
Course Hours:	56	**Course GPA Weighting:**	4
Prerequisite:	N/A		
Corequisite:	N/A		
Laptop Course:	**Yes** [ ] **No** [X]		
Delivery Mode(s):	**In class** [ ] **Online** [X] **Hybrid** [ ] **Correspondence** [ ]		

Pandemic remote teaching delivery mode	[ ] **Fully asynchronous**	[X] **Combined asynchronous and synchronous**	
Remote proctoring required	**Yes** [ ]	**No** [X]	
Authorized by (Dean or Director):	Rebecca Milburn	**Date:**	May 2021

Prepared by		
First Name	**Last Name**	**Email**
Louis	Bertrand	louis.bertrand@durhamcollege.ca
Phillip	Jarvis	phillip.jarvis@durhamcollege.ca

This course supports the following program(s) and program learning outcomes.

BMTY: Biomedical Engineering Technology	#1. Communicate information effectively, credibly, and accurately by analyzing, interpreting, and producing electrical and electronics drawings and other related documents and graphics.
	#3. Select and use a variety of troubleshooting techniques and test equipment to assess electronics circuits, equipment, systems and subsystems.
	#4. Design, build, and troubleshoot working prototypes of electronics circuits, equipment, systems, and subsystems to meet job requirements, functional specifications and relevant standards;
	#5. Modify, maintain and repair electronics equipment and systems to ensure that they function properly.
	#6. Select for purchase electronics equipment, components, and systems that fulfill the job requirements and functional specifications;
	#7. Design, analyze and troubleshoot logic and digital circuits.
	#10. Design, analyze and troubleshoot microprocessor-based systems.
	#14. Apply knowledge of basic shop practices to electronics engineering workplaces.
ELTC: Electronics Engineering Technician	#1. Analyze, interpret, modify and prepare electrical and electronics drawings, layouts and reports, with guidance as required.
	#2. Analyze and solve routine technical problems related to electronics engineering by applying fundamental concepts of mathematics and science.
	#4. Assemble, modify, test and troubleshoot electronic circuits, equipment and systems in accordance with job requirements, functional specifications and relevant standards, with guidance as required.
	#7. Analyze and troubleshoot logic and digital circuits, as well as embedded microprocessor-based and microcontroller-based systems, including assembly and high-level language programs.
	#9. Analyze and troubleshoot circuits consisting of low power, high power, active and electromechanical components, and analog integrated circuits.
	#12. Apply relevant shop practices in compliance with safety policies and current regulations for electronics engineering workplaces.
ELTY: Electronics Engineering Technology	#1. Analyze, interpret, modify, design and produce electrical and electronics drawings, layouts and reports.
	#2. Analyze and solve technical problems related to electronics engineering by applying principles of advanced mathematics and science.
	#4. Design, build, test and troubleshoot electronic circuits, equipment, systems and subsystems in accordance with job requirements, functional specifications and relevant standards.
	#7. Design, modify, analyze and troubleshoot logic and digital circuits, and embedded microprocessor-based and microcontroller-based systems, including assembly and high-level language programs.
	#12. Apply relevant shop practices in compliance with safety policies and current regulations for electronics engineering workplaces.
	#14. Complete work in compliance with relevant legislation, established standards, policies, procedures and regulations, and ethical principles.
	#15. Contribute to the planning, implementation, management and evaluation of team projects by applying project management

principles.

Course Description:

This course introduces the student to the broad topic of digital electronics and hardware-software digital systems. Starting with a theoretical foundation in Boolean logic, binary arithmetic, combinational and sequential circuits, the course develops a comprehensive overview of the technologies used to implement logic functions, namely discrete electronics, field programmable gate arrays (FPGA) and microcontrollers (MCU). The course also offers a brief overview of logic synthesis using the Verilog hardware description language. Extensive use of simulation software allows students to observe the behaviour of logic networks and predict outcomes. Troubleshooting is integral to the course - students are expected to identify and correct design problems, wiring faults, programming errors and software misconfigurations. In the laboratory, students will assemble circuits on prototyping boards and program and test digital functions with a variety of technologies including FPGAs and MCU. Students will demonstrate their understanding of the subject matter with a practical project at the end of the course.

Campus Closure Notice

In the event of a campus closure during which time classes cannot be conducted or attended in person, course delivery will be conducted remotely where possible. Should teaching and learning resume on campus, students may be organized into smaller groups for classroom delivery, in accordance with directions from public health authorities. In either situation, the learning plan sequence and/or evaluation methods may be adjusted to address topics requiring hands-on, practical learning activities.

Subject Eligibility for Prior Learning Assessment & Recognition (PLAR):

Prior Learning Assessment and Recognition (PLAR) is a process a student can use to gain college credit(s) for learning and skills acquired through previous life and work experiences. Candidates who successfully meet the course learning outcomes of a specific course may be granted credit based on the successful assessment of their prior learning. The type of assessment method (s) used will be determined by subject matter experts. Grades received for the PLAR challenge will be included in the calculation of a student's grade point average.

The PLAR application process is outlined in http://www.durhamcollege.ca/plar. Full-time and part-time students must adhere to all deadline dates. Please email: PLAR@durhamcollege.ca for details.

PLAR Eligibility

Yes [X] **No** [ ]

PLAR Assessment (if eligible):

- [ ] Assignment
- [X] Exam
- [X] Portfolio
- [X] Other

Complete a project that includes the major elements of the course.

Course Learning Outcomes

Course Learning Outcomes contribute to the achievement of Program Learning Outcomes for courses that lead to a credential (e.g. diploma). A complete list of Vocational/Program Learning Outcomes and Essential Employability Skill Outcomes are located in each Program Guide.

Course Specific Learning Outcomes (CLO)

Student receiving a credit for this course will have reliably demonstrated their ability to:

CLO1	Describe analogue and digital signal characteristics and perform input/output timing analysis in electric circuits containing switches.
CLO2	Understand number systems and convert numbers from one system to another to find the equivalent values.
CLO3	Describe the functioning of various fundamental combinational and sequential components of digital circuits and write truth tables and the corresponding Boolean equations.
CLO4	Solve Boolean equations for a given circuit using simplification techniques namely Boolean algebra and Karnaugh map techniques.
CLO5	Use manufacturers' data sheets, application notes and other sources of technical information to design digital circuits.
CLO6	Write truth tables for a given digital control problem to develop a Boolean equation that leads to a functional simplified digital circuit and verify the circuit functions by simulation models.
CLO7	Verify the functioning of various digital circuits by wiring on breadboards in the laboratory and also by developing simulation models using Proteus software.
CLO8	Communicate the results and observations of laboratory work clearly with industry standard terminology.
CLO9	Generate timing waveforms to relate the functioning of counters and flip-flops using gates and FPGAs.
CLO10	Understand the basic concepts of microcontrollers and FPGAs to develop simple applications.

Essential Employability Skill Outcomes (ESSO)

This course will contribute to the achievement of the following Essential Employability Skills:

- [X] EES 1. Communicate clearly, concisely and correctly in the written, spoken, and visual form that fulfills the purpose and meets the needs of the audience.
- [X] EES 2. Respond to written, spoken, or visual messages in a manner that ensures effective communication.
- [X] EES 3. Execute mathematical operations accurately.
- [X] EES 4. Apply a systematic approach to solve problems.
- [X] EES 5. Use a variety of thinking skills to anticipate and solve problems.
- [ ] EES 6. Locate, select, organize, and document information using appropriate technology and information systems.
- [X] EES 7. Analyze, evaluate, and apply relevant information from a variety of sources.
- [ ] EES 8. Show respect for the diverse opinions, values, belief systems, and contribution of others.
- [ ] EES 9. Interact with others in groups or teams in ways that contribute to effective working relationships and the achievement of goals.
- [X] EES 10. Manage the use of time and other resources to complete projects.
- [X] EES 11. Take responsibility for one's own actions, decisions, and consequences.

Evaluation Criteria:

The Course Learning Outcomes and Essential Employability Skills Outcomes are evaluated by the following evaluation criterion.

Evaluation Description	Course Learning Outcomes	EESOs	Weighting
Quiz: 1: intro, logic gates, truth tables [Evaluation note 1]	CLO1, CLO2, CLO3, CLO6	EES1, EES3, EES4, EES5, EES7	5
Quiz: 2: Flip-flops, FPGA intro [Evaluation notes 1, 4]	CLO3, CLO4, CLO6, CLO9	EES1, EES3, EES4, EES5, EES7	5
Test: 1: Combinational logic networks, minimization, Karnaugh maps [Evaluation notes 2, 4]	CLO1, CLO2, CLO3, CLO4, CLO6	EES1, EES3, EES4, EES5, EES7	15
Test: 2: Sequential logic networks, FPGA, microcontrollers [Evaluation notes 2, 4]	CLO1, CLO2, CLO3, CLO4, CLO6, CLO8, CLO9, CLO10	EES3, EES4, EES5, EES7, EES10	15
Lab Activity: Eight labs (+ Lab 0 Intro) throughout the semester [Evaluation notes 4, 5, 6, 7, 8]	CLO1, CLO2, CLO3, CLO4, CLO5, CLO6, CLO7, CLO8, CLO9, CLO10	EES1, EES2, EES3, EES4, EES5, EES7, EES10, EES11	40
Project: integrating the theory, techniques and devices encountered throughout the course.	CLO1, CLO2, CLO3, CLO4, CLO5, CLO6, CLO7, CLO8, CLO9, CLO10	EES1, EES2, EES3, EES4, EES5, EES7, EES10, EES11	20
Total			**100%**

Notes:

1. Quiz format: short answer, multiple choice.
2. Test format: short answer, multiple choice, problem solving and drawing circuit schematics, performing simulations.
3. Test and quiz for pandemic contingency: tests and quizzes will be conducted online through DC Connect, using the Quiz and Assignment pages. During tests and quizzes, an online "meeting" session will stay open for instructions and questions.
4. Students who unavoidably miss a test, quiz, lab or other evaluation must notify the professor in advance of the scheduled evaluation. No personal details are required (i.e. no doctor's note). Students missing an evaluation must complete the evaluation promptly, typically before the end of the following week. Students who miss more than one opportunity to complete the evaluation may receive a zero (0) grade for that evaluation, at the professor's discretion.
5. There are 8 mandatory labs, each worth 5%. Lab 0 is an optional introductory lab and the grade counts as a bonus. Lab activities are done individually and each student will submit her/his own report.
6. Labs consist of schematic entry, simulation, firmware development (flowcharts), device programming, prototyping board assembly and troubleshooting, and measurements and observations. A structured lab report format will be published for each lab activity. For online labs during pandemic measures, screen captures, smartphone or webcam videos are required to demonstrate the completed lab assignment.
7. The due date for each lab assignment will be at the start of the next lab or as announced when the lab is issued (consult DC Connect calendar). Late submissions are subject to 10% penalty within the week in which the report is due and 20% penalty in the next week. Beyond the second week, the grade will be zero (0). The resulting grade is calculated as resulting = grade * (1 - percent_penalty), where percent_penalty has a value of 0.1 or 0.2.

8. Students must show (photo or scan) proof of purchase for the DGFN1131 parts kit otherwise lab assignments 0 (Introduction) and 1 (AND gate) will receive a grade of zero; without the lab kit, students will experience significant difficulty in completing the lab assignments.

Required Text(s) and Supplies:

1. DGFN 1131 Lab Kit - Must be purchased at the beginning of the semester from recommended vendor. The link is posted on DC Connect.

Recommended Resources (purchase is optional):

N/A

Policies and Expectations for the Learning Environment:

General Policies and Expectations:

General College policies related to	General policies related to
+ Acceptable Use of Information Technology	+ attendance
+ Academic Policies	+ absence related to tests or assignment due dates
+ Academic Honesty	+ excused absences
+ Student Code of Conduct	+ writing tests and assignments
+ Students' Rights and Responsibilities can be found on-line at http://www.durhamcollege.ca/academicpolicies	+ classroom management can be found in the Program Guide (full time programs only) in MyCampus http://www.durhamcollege.ca/mycampus/

Course Specific Policies and Expectations:

Lecture sessions (online or in-class after pandemic measures cancelled) are mandatory. Students missing the lecture are responsible for catching up with the material on their own.

Lab activities (online or in-class after pandemic measures cancelled) are mandatory. Students missing more than three lab assignments may receive a formal Academic Notice that may trigger follow up actions from the School of Science and Technology.

Electrostatic discharge (ESD) may cause unseen damage to integrated circuits and other electronic devices. Students are responsible for wearing a grounded antistatic wrist strap and working on an antistatic work surface while handling electronic devices and assemblies.

Students are responsible for the parts kit and its contents. Missing parts must be reported within one day of receiving the kit (an inventory form will be provided). Damaged or lost parts are the responsibility of the student. Replacements may be purchased by the student from the college or from external vendors.

General Course Outline Notes:

1. Students should use the course outline as a learning tool to guide their achievement of the learning outcomes for this course. Specific questions should be directed to their individual professor.
2. The college considers the electronic communication methods (i.e. DC Mail or DC Connect) as the primary channel of communication. Students should check the sources regularly for current course information.
3. Professors are responsible for following this outline and facilitating the learning as detailed in this outline.
4. Course outlines should be retained for future needs (i.e. university credits, transfer of credits etc.)
5. A full description of the Academic Appeals Process can be found at https://durhamcollege.ca/about/governance/policies/academic-policies .
6. Faculty are committed to ensuring accessible learning for all students. Students who would like assistance with academic access and accommodations in accordance with the Ontario Human Rights Code should register with the Access and Support Centre (ASC). ASC is located in room SW116, Oshawa Campus and in room 180 at the Whitby Campus. Contact ASC at 905-721-3123 for more information.
7. Durham College is committed to the fundamental values of preserving academic integrity. Durham College and faculty members reserve the right to use electronic means to detect and help prevent plagiarism. Students agree that by taking this course all assignments could be subject to submission either by themselves or by the faculty member for a review of textual similarity to Turnitin.com. Further information about Turnitin can be found on the Turnitin.com Web site.

Learning Plan

The Learning Plan is a planning guideline. Actual delivery of content may vary with circumstances.

Students will be notified in writing of changes that involve the addition or deletion of learning outcomes or evaluations, prior to changes being implemented, as specified in the Course Outline Policy and Procedure at Durham College.

Wk.	**Hours:** 4 **Delivery:** Online
1	**Course Learning Outcomes** CLO1, CLO2, CLO3, CLO6, CLO10
	Essential Employability Skills **Taught:** EES3, EES4 **Practiced:** EES3, EES4, EES5, EES7, EES10
	Intended Learning Objectives Introduction: digital technologies, analog vs. digital, continuous vs. sampled, Boolean logic, Boolean algebra, Venn diagrams, unsigned binary numbering, ways of representing digital electronic device operation. Basic gates - AND, OR, NOT, NAND, NOR
	Intended Learning Activities Lecture: introduction to course, introduction to digital technologies, digital theory Lab 0: Install and license Proteus design software; perform introductory Lab 0 (flowcharts in Proteus Visual Designer); submit observations and screen captures to DC Connect.
	Resources and References Week 1 lecture material; Proteus installation and licensing instructions; Lab 0 instructions and starter file.
	Evaluation Lab Activity: Eight labs (+ Lab 0 Intro) throughout the semester [Evaluation notes 4, 5, 6, 7]

Wk.	Hours: 4 Delivery: Online
2	**Course Learning Outcomes** CLO1, CLO2, CLO3, CLO5, CLO6, CLO7, CLO8
	Essential Employability Skills **Taught:** EES3, EES4 **Practiced:** EES3, EES4, EES5, EES7
	Intended Learning Objectives Discrete logic ICs - power; breadboard power module; (VDD=3V3) and GND - Logic levels high/low; ESD awareness, antistatic gear
	Intended Learning Activities Lecture: Logic with discrete integrated circuits; Powering circuits; ESD awareness Lab 0: Install and license Proteus design software; perform introductory Lab 0 (flowcharts in Proteus Visual Designer); submit observations and screen captures to DC Connect. (continued from week 1 if not already done)
	Resources and References Week 2 lecture material; Proteus installation and licensing instructions; Lab 0 instructions and starter file.
	Evaluation Lab Activity: Eight labs (+ Lab 0 Intro) throughout the semester [Evaluation notes 4, 5, 6, 7]
Wk.	**Hours:** 4 **Delivery:** Online
3	**Course Learning Outcomes** CLO2, CLO3, CLO4, CLO5, CLO6, CLO7, CLO8
	Essential Employability Skills **Taught:** EES3, EES4 **Practiced:** EES3, EES4, EES5, EES7
	Intended Learning Objectives Basic gates XOR, XNOR; applications: comparison, parity, error detection and correction, stream cipher
	Intended Learning Activities Lecture: Basic gates XOR, XNOR and applications Lab 1: Logic ICs on breadboard; inputs, outputs, indicators, power and ground supplies; AND, OR, NOT gate operation.
	Resources and References Week 3 lecture material; Lab 1 instructions and report template
	Evaluation **Weighting** Lab Activity: Eight labs (+ Lab 0 Intro) throughout the semester 5% [Evaluation notes 4, 5, 6, 7]

Wk.	Hours: 4 Delivery: Online
4	**Course Learning Outcomes** CLO3, CLO4, CLO5, CLO6, CLO7, CLO8
	Essential Employability Skills **Taught:** EES3, EES4 **Practiced:** EES3, EES4, EES5, EES7
	Intended Learning Objectives Boolean algebra De Morgan's theorem and complements of NAND-NOR functions Sum-of-products / product-of-sums Venn diagrams with 3 sets (inputs); Application of 3-input network: 2-1 multiplexer. Practical skills: schematic diagrams; placement diagrams.
	Intended Learning Activities Lecture: Boolean algebra Exercises: Boolean algebra problems Quiz 1: Basic gates Lab 2: XOR applications.
	Resources and References Week 4 lecture material; Lab 2 instructions and report template
	Evaluation **Weighting** Lab Activity: Eight labs (+ Lab 0 Intro) throughout the semester 5% [Evaluation notes 4, 5, 6, 7, 8]
Wk.	**Hours:** 4 **Delivery:** Online
5	**Course Learning Outcomes** CLO2, CLO3, CLO4, CLO5, CLO6, CLO8, CLO10
	Essential Employability Skills **Taught:** EES3, EES4 **Practiced:** EES3, EES4, EES5, EES7
	Intended Learning Objectives Intro to logic with microcontrollers Setup and loop functions; GPIO pins: mode input/output, read, write; Pull-up vs. pull-down, negative logic.
	Intended Learning Activities Lecture: Logic operation with microcontrollers. Quiz 1: intro, logic gates, truth tables Lab 3: Functions of three inputs; 2-1 multiplexer Practical skills: schematic diagrams; placement diagrams.
	Resources and References Week 5 lecture material; Lab 3 instructions and report template
	Evaluation **Weighting** Quiz: 1: intro, logic gates, truth tables [Evaluation note 1] 10% Lab Activity: Eight labs (+ Lab 0 Intro) throughout the semester [Evaluation notes 4, 5, 6, 7]

Wk.	Hours: 4 Delivery: Online
6	**Course Learning Outcomes** CLO1, CLO3, CLO4
	Essential Employability Skills **Taught:** EES2, EES3, EES4, EES5 **Practiced:** EES3, EES4, EES5, EES7, EES10, EES11
	Intended Learning Objectives Logic minimization with Boolean algebra and Karnaugh maps; Timing diagrams and 1 -> 0 -> 1 notation on schematics
	Intended Learning Activities Lecture: logic minimization Exercises: logic minimization Lab 4: Microcontrollers - logic functions with Proteus Visual Designer - three light switches in the gym problem.
	Resources and References Week 6 lecture material; Lab 4 instructions, starter file and report template
	Evaluation Lab Activity: Eight labs (+ Lab 0 Intro) throughout the semester [Evaluation notes 4, 5, 6, 7]
Wk.	**Hours:** 4 **Delivery:** Online
7	**Course Learning Outcomes** CLO1, CLO3, CLO4, CLO5, CLO6, CLO7, CLO8, CLO10
	Essential Employability Skills **Taught:** EES3, EES4 **Practiced:** EES3, EES4, EES5, EES7
	Intended Learning Objectives Test 1: Summative evaluation weeks 1-6
	Intended Learning Activities Test 1: Boolean logic theory and combinational logic networks Lab 4: Microcontrollers - continued from week 6.
	Resources and References Test 1 review; Lab 4 instructions, starter file and report template
	Evaluation **Weighting** Test: 1: Combinational logic networks, minimization, Karnaugh maps 20% [Evaluation notes 2, 4] Lab Activity: Eight labs (+ Lab 0 Intro) throughout the semester [Evaluation notes 4, 5, 6, 7]

Wk.	Hours: 4	Delivery: Online
8	**Course Learning Outcomes** CLO2, CLO3, CLO4, CLO5, CLO6, CLO7, CLO8, CLO9, CLO10	
	Essential Employability Skills **Taught:** EES3, EES4	**Practiced:** EES3, EES4, EES5, EES7, EES11
	Intended Learning Objectives Programmable logic: AND-OR network, FPGA with lookup tables. Sequential circuits: memory, concept of the state of a system; SR latch, gated SR latch Concept of a clock signal Edge triggered D flip-flops Toggle flip-flops Debounce edge triggered inputs	
	Intended Learning Activities Lecture: programmable logic basics; sequential logic; latches; synchronous sequential circuits Lab 5: Intro to FPGAs with IceStudio and TinyFPGA BX. Install IceStudio, install TinyFPGA programmer (software on Windows 10).	
	Resources and References Week 8, 9 lecture material; IceStudio documentation; Lab 5 instructions, starter file and report template	
	Evaluation Lab Activity: Eight labs (+ Lab 0 Intro) throughout the semester [Evaluation notes 4, 5, 6, 7]	**Weighting** 5%
Wk.	**Hours:** 4	**Delivery:** Online
9	**Course Learning Outcomes** CLO2, CLO3, CLO4, CLO5, CLO6, CLO7, CLO8, CLO9, CLO10	
	Essential Employability Skills **Taught:** EES3, EES4, EES5	**Practiced:** EES3, EES4, EES5, EES7
	Intended Learning Objectives Sequential circuits (continued from week 8)	
	Intended Learning Activities Lecture: sequential logic; latches; synchronous sequential circuits (continued from week 8); Lab 6: D flip-flop with FPGA; motor controller problem.	
	Resources and References Week 8, 9 lecture material; IceStudio documentation; Lab 6 instructions, starter file and report template	
	Evaluation Lab Activity: Eight labs (+ Lab 0 Intro) throughout the semester [Evaluation notes 4, 5, 6, 7]	**Weighting** 5%

Wk.	Hours: 4	Delivery: Online
10	**Course Learning Outcomes** CLO2, CLO3, CLO4, CLO5, CLO6, CLO7, CLO8, CLO10	
	Essential Employability Skills **Taught:** EES3, EES4	**Practiced:** EES3, EES4, EES5, EES7
	Intended Learning Objectives Binary arithmetic with unsigned integers; carry bit; arithmetic overflow. Arithmetic circuits: half and full adder.	
	Intended Learning Activities Lecture: unsigned binary arithmetic Quiz 2: flip-flops and FPGA intro Lab 7: D flip-flop with microcontroller (Proteus with Visual Designer); motor controller problem.	
	Resources and References Week 10, 11 lecture material; Lab 7 instructions, starter file and report template	
	Evaluation Quiz: 2: Flip-flops, FPGA intro [Evaluation notes 1, 4] Lab Activity: Eight labs (+ Lab 0 Intro) throughout the semester [Evaluation notes 4, 5, 6, 7]	**Weighting** 10%

Wk.	Hours: 4	Delivery: Online
11	**Course Learning Outcomes** CLO2, CLO3, CLO4, CLO5, CLO6, CLO7, CLO8, CLO10	
	Essential Employability Skills **Taught:** EES3, EES4	**Practiced:** EES3, EES4, EES5, EES7
	Intended Learning Objectives Binary arithmetic and arithmetic circuits (continued from week 10). Hexadecimal numbering.	
	Intended Learning Activities Lecture: unsigned binary arithmetic; hexadecimal numbering. Lab 8: 4 bit adder with MSI logic and FPGA.	
	Resources and References Week 10, 11 lecture material; Lab 8 instructions, starter files and report template	
	Evaluation Lab Activity: Eight labs (+ Lab 0 Intro) throughout the semester [Evaluation notes 4, 5, 6, 7]	**Weighting** 5%

Wk.	Hours: 4 Delivery: Online
12	**Course Learning Outcomes** CLO1, CLO2, CLO3, CLO4, CLO5, CLO6, CLO7, CLO8, CLO9, CLO10
	Essential Employability Skills **Taught:** EES3, EES4 **Practiced:** EES3, EES4, EES5, EES7, EES10, EES11
	Intended Learning Objectives Digital technologies overview
	Intended Learning Activities Project introduction Combinational and sequential logic system with discrete logic devices and TinyFPGA.
	Resources and References Project instructions and starter files.
	Evaluation
Wk.	**Hours:** 4 **Delivery:** Online
13	**Course Learning Outcomes** CLO1, CLO2, CLO3, CLO4, CLO5, CLO6, CLO7, CLO8, CLO9, CLO10
	Essential Employability Skills **Taught:** EES3, EES4 **Practiced:** EES3, EES4, EES5, EES7, EES10, EES11
	Intended Learning Objectives Summative evaluation weeks 8-12
	Intended Learning Activities No lecture planned Test 2: sequential logic, FPGA, microcontrollers.
	Resources and References Test 2 review; project instructions and starter files.
	Evaluation **Weighting** Test: 2: Sequential logic networks, FPGA, microcontrollers [Evaluation notes 2, 4] 15%

Wk.	Hours: 4 Delivery: Online
14	**Course Learning Outcomes** CLO1, CLO2, CLO3, CLO4, CLO5, CLO6, CLO7, CLO8, CLO9, CLO10
	Essential Employability Skills **Taught:** EES3, EES4 **Practiced:** EES3, EES4, EES5, EES7, EES10, EES11
	Intended Learning Objectives Digital technologies overview
	Intended Learning Activities Project: combinational and sequential logic system with discrete logic devices and TinyFPGA. No lecture planned; time reserved for project work. Project due Friday midnight of week 14.
	Resources and References Project instructions and starter files.
	Evaluation **Weighting** Project: integrating the theory, techniques and devices encountered throughout the course. 20%